WHAT IS CLAIMED IS:

1. An apparatus comprising an integrated circuit which includes:

an insulating layer; and

a group of at least two elongate runs which are electrically conductive, which are electrically separate from each other, which each extend approximately in a direction, and which each have along the length thereof alternating first and second portions that are electrically coupled by third portions, said first portions of said runs being located on a side of said insulating layer opposite from said second portions thereof, and said third portions having sections which extend through said insulating layer;

wherein for substantially each point along each of said first and second portions of each of said runs, a plane perpendicular to said direction and containing that point intersects a respective different point of every other said run, each pair of adjacent said points in said plane being points which are respectively located on opposite sides of said insulating layer.

2. An apparatus according to Claim 1, wherein for each said run, a cumulative amount of material in said first portions thereof conforms to a predetermined ratio in relation to a cumulative amount of material in said second portions thereof.

3. An apparatus according to Claim 2, wherein said predetermined ratio is substantially 1:1.

4. An apparatus according to Claim 1, wherein said runs each extend substantially parallel to said direction and substantially parallel to each other along the entire length thereof.

5. An apparatus according to Claim 1, wherein at least one of said first portions of each said run crosses over one of said second portions of another of said runs.

6. An apparatus according to Claim 5, wherein said runs of said group includes first, second, third and fourth runs, said first and second runs each having at least one of said first portions thereof arranged to cross over one of said second portions of the other thereof, said third and fourth runs each having at least one of said first portions thereof arranged to cross over one of said second portions of the other thereof, and said first and second runs each having a respective said third portion thereof aligned with each said crossover of said third and fourth runs.

7. An apparatus according to Claim 6, wherein said third and fourth runs each have a respective said third portion thereof aligned with each said crossover of said first and second runs.

8. An apparatus according to Claim 5, wherein each said run is routed in a stairstep manner across other said runs until an outer side of said group is reached, and then is routed in a stairstep manner back across other said runs toward an opposite side of said group.

9. An apparatus according to Claim 8, wherein said third portions of each said run are located where that run is at one of the outer sides of said group.

10. An apparatus according to Claim 5, wherein each said run is routed in a stairstep manner across other said runs until an outer side of said group is reached, and then is routed in a stairstep manner back across other said runs toward an opposite side of said group, each said run being free of said third portions thereof at locations where that run reaches either outer side of said group, said third portions of each said run being located adjacent one of said crossovers of that run in approximate alignment with one of said locations where another said run reaches either outer side of said group.

11. An apparatus according to Claim 1, wherein said integrated circuit includes an array of memory cells, each of said cells being electrically coupled to one of said runs.

12. An apparatus according to Claim 1, wherein said integrated circuit includes an array of memory cells, each of said cells being electrically coupled to two of said runs.

13. An apparatus according to Claim 12, wherein said integrated circuit includes a sense amplifier, and includes a plurality of selectively actuatable electronic switches which each couple said sense amplifier to a respective one said runs of said group.

14. An apparatus according to Claim 1, wherein a segment of one of said two elongate runs is disposed on the same side of said insulating layer as a segment of the other of said two elongate runs, each said segment being part of a respective said third portion of a respective one of said two elongate runs, and including on a side of said insulating layer opposite from said segments a further run which is separate from said runs of said group.

15. A method of making an integrated circuit having an insulating layer and a group of at least two elongate runs which are electrically conductive, which are electrically separate from each other, and which each extend approximately in a direction, comprising the steps of:

configuring each of said runs to have along the length thereof alternating first and second portions that are electrically coupled by third portions;

locating said first portions of each of said runs on a side of said insulating layer opposite from said second portions thereof in a manner so that, for substantially each point along each of said first and second portions of each of said runs, a plane perpendicular to said direction and containing that point intersects a respective different point of every other said run, each pair of adjacent said points in said plane being points which are respectively located on opposite sides of said insulating layer; and

fabricating conductive sections which each extend through said insulating layer, each of said third portions including one of said sections.

16. A method according to Claim 15, wherein said configuring step includes the step of configuring said first and second portions so that, for each said run, a cumulative amount of material in said first portions thereof conforms to a predetermined ratio in relation to a cumulative amount of material in said second portions thereof.

17. A method according to Claim 16, including the step of selecting a ratio of 1:1 as said predetermined ratio.

18. A method according to Claim 15, including the step of routing said runs so that said runs each extend substantially parallel to said direction and substantially parallel to said each other along the entire length thereof.

19. A method according to Claim 15, including the step of routing said runs so that at least one of said first portions of each said run crosses over one of said second portions of another of said runs.

20. A method according to Claim 19, wherein said routing step includes the step of routing first and second runs of said group so that they each have at least one of said first portions thereof arranged to cross over one of said second portions of the other thereof, and includes the step of routing said third and fourth runs so that they each have at least one of said first portions thereof arranged to cross over one of said second portions of the other thereof, and wherein said fabricating step is carried out by locating a respective said third portion of each of said first and second runs in alignment with a respective said crossover of said third and fourth runs, and locating a respective said third portion of each of said third and fourth runs in alignment with a respective said crossover of said first and second runs.

21. A method according to Claim 19, wherein said routing step includes the step of routing each of said runs in a stairstep manner across other said runs until an outer side of said group is reached, and then routing that run in a stairstep manner back across other said runs toward an opposite side of said group, and wherein said fabricating step is carried out by locating said third portions of each said run where that run is at one of the outer sides of said group.

22. A method according to Claim 19, wherein said routing step includes the step of routing each said run in a stairstep manner across other said runs until an outer side of said group is reached, and then routing that run in a stairstep manner back across other said runs toward an opposite side of said group, and wherein said fabricating step includes the step of keeping each said run free of said third portions at locations where that runs reaches either outer side of said group, and locating a respective said third portion of each said run adjacent one of said crossovers of that run and in approximate alignment with one of the locations where another said run reaches either outer side of said group.

23. A method according to Claim 15, wherein said integrated circuit includes an array of memory cells, and including the step of electrically coupling each said memory cell to two of said runs.

24. A method according to Claim 23, including the step of coupling each of said runs to a sense amplifier of said integrated circuit through a respective electronic switch of said integrated circuit.